IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application No.: 10/821,412	§	Examiner:	Eland, Shawn
Filed: April 9, 2004	§	Group/Art Unit:	2188
Inventor(s):	§	Atty. Dkt. No:	5681-01601
Landin, et al.	§	Confirm No.	8427
	§		
	§		
	§		
Title: MULTI-NODE	§		
COMPUTER SYSTEM	§		
EMPLOYING A	§		
REPORTING	§		
MECHANISM FOR	§		
MULTI-NODE	§		
TRANSACTIONS	§		

REPLY BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

In response to the Examiner's answer of July 9, 2008, Appellant presents this Reply Brief.

Appellant uses the same headings below that were used in the Appeal Brief, to reply to various arguments in the Answer. Appellant respectfully requests that this appeal be considered by the Board of Patent Appeals and Interferences.

VII. ARGUMENT

First Ground of Rejection:

Claims 1, 14, and 26

In the response to arguments section of the Examiner's Answer dated July 9, 2008, the Examiner alleges that the cache memory of Liencres is "interconnected" through element 32, from which the memory 37 and the processor 21 are part of so the bus 33 does fit within the claim language." Appellant disagrees. As previously argued, Appellant further maintains that, even if, *arguendo*, one were to suppose that the cache memory 37 were analogous to the Appellant's claimed system memory, the topology of Liencres is different. Specifically, as is plainly evident in the drawings, the cache memory 37 is ***not*** coupled to the bus 33 but is instead coupled to the cache controller 35 and to processor 21 by a separate bus. As such, the bus cache controller 31, the processor 21 and the cache memory 37 are NOT all coupled together by bus 33 as suggested by the Examiner and required by Appellant's claims. Thus, Appellant fails to see how the system of Liencres teaches the structure recited in Appellant's claims. Appellant submits it does not.

The Examiner further alleges in the response to arguments section of the Examiner's Answer dated July 9, 2008, "A lock manager is not necessary... the transaction cannot be satisfied if a write time is published after the start of the read, thus invalidating the data. Starting the process is OK, but when the report is published before the read is complete, the transaction cannot be satisfied. The report includes the write time sent out by another node so it is definitely not the requested data."

However, as previously pointed out in the Appeal Brief, and whether or not a lock manager is used, the Examiner acknowledges the "report" of Chandrasekaran is sent by an agent or process in another node that writes the data. Clearly, Appellant's claim requires 'a node including an active device" and "wherein in response to receiving **from the active device** an address packet initiating a transaction to gain an access right to a coherency unit, **the system memory** is configured to **send a report** corresponding to the

address packet to the interface **if the transaction cannot be satisfied within the node**."

Again, Appellant submits Chandrasekaran does not teach an active device within the node initiating the request, and the memory within the node responding with a report if the transaction cannot be satisfied. Further, Chandrasekaran does not teach the interface within the node, ignoring the address packet and instead sending a coherency message to another node.

Accordingly, Appellant respectfully submits that each of claims 1, 14, and 26 recites a combination of features not taught or suggested in Liencres, Chandrasekaran, or Roy. For example, claim 1 recites a combination of features including:

> a node including an active device, an interface to an inter-node network, a system memory, and an address network and a data network that is separate from the address network, coupling the active device, the interface, and the memory;
>
> ...
>
> wherein in response to receiving **from the active device** an address packet initiating a transaction to gain an access right to a coherency unit, the **system memory** is configured to **send a report** corresponding to the address packet to the interface **if the transaction cannot be satisfied within the node**;
>
> wherein the interface is configured to ignore the address packet and to send a coherency message requesting the access right to the additional node via the inter-node network in response to the report. (Emphasis added).

These features are not taught or suggested either singly or in combination by the cited references.

Separately argued dependent claims

Claims 3, 16 and 28

In the response to arguments section of the Examiner's Answer dated July 9, 2008, the Examiner alleges that "[t]he 'modified access state' is just another way of saying having full write access" and "a global access state other than a modified global access state means that another mode currently owns the coherency unit and will send a

its write report after it finishes writing." Appellant submits the write report of Chandrasekaran is not the same as the report sent by the memory as recited in Appellant's claims. Clearly, a node (silent on which device) sending a write report including a time stamp, in response to writing data, as in Chandrasekaran, is different than a memory sending a report in response to not being able to satisfy the transaction request. This is even emphasized further by the fact that the request is an RTO transaction by an active device in a node in which the coherency unit is not in the Modified global access state. It has nothing to do with the writing device sending a time stamp.

Appellant further submits the recited language is also not taught by Liencres, as previously argued in the Appeal Brief filed May 27, 2008.

Claims 3, 16 and 28 depend from claims 1, 14 and 26, respectively. Accordingly, the rejection of claims 3, 16 and 28 is in error for at least the reasons highlighted above with regard to claims 1, 14 and 26. Additionally, each of claims 3, 16 and 28 recite a combination of features including: "wherein the address packet is a read-to-own packet, the access right is a write access right, and wherein the system memory is configured to send the report corresponding to the read-to-own packet to the interface if a global access state of the coherency unit in the node is any global access state other than a modified global access state" which are not taught or suggested by the cited references.

Appellant submits claims 16 and 28 recite similar features. Thus, for at least the above stated reasons, Appellant submits that the rejection of claims 16 and 28 is in error and requests reversal of the rejection.

CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejection of claims 1-38 is erroneous, and reversal of his decision is respectfully requested.

The Commissioner is authorized to charge any fees that may be due to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-01601/SJC.

Respectfully submitted,

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